HMC320MS8G

GaAs MMIC LOW NOISE AMPLIFIER , 5.0 - 6.0 GHz

Typical Applications

The HMC320MS8G is ideal for:

• UNII

• HiperLAN

Features

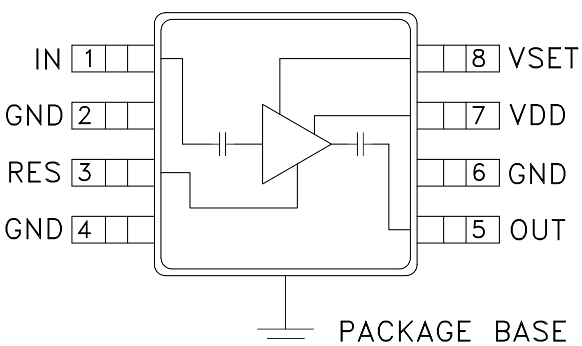
Selectable Functionality:
LNA, Driver, or LO Buffer Amp

Adjustable Input IP3 Up to +10 dBm

+3V Operation

Ultra Small 8 Lead MSOP:
14.8 mm² x 1mm High

Functional Diagram



General Description

The HMC320MS8G is a low cost C-band fixed gain Low Noise Amplifier (LNA). The HMC320MS8G operates using a single positive supply that can be set between +3V and +5V. With +3V bias, the LNA provides a noise figure of 2.5dB, 12dB gain and better than 10dB return loss across the UNII band. The HMC320MS8G also features adaptive baising that allows the user to select the optimal P1dB performance for their system using an external set resistor on the “RES” pin. P1dB performance can be set between a range of +1 dBm to +13dBm. The low cost LNA uses an 8-leaded MSOP ground base surface mount plastic package, which occupies less than 14.8mm².

Electrical Specifications, T_A = +25° C, Vdd = +3V

Parameter	Low Power* (VSET = 0V, Idd = 7 mA)			Medium Power* (VSET = 3V, Idd = 25 mA)			High Power* (VSET = 3V, Idd = 40 mA)			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range		5 - 6			5 - 6			5 - 6		GHz
Gain	8	10	16	8	12	16	9	13	16	dB
Gain Variation over Temperature		0.025	0.035		0.025	0.035		0.025	0.035	dB/°C
Gain Flatness		±0.5			±1.0			±1.5		dB
Noise Figure		2.7	3.8		2.5	3.8		2.6	3.8	dB
Input Return Loss	4	10		4	10		4	10		dB
Output Return Loss	7	13		10	18		10	20		dB
Output Power for 1 dB Compression (P1dB)	-4	-1		6	9		9	12		dBm
Input Third Order Intercept Point (IIP3)	-3	1		4	8		6	10		dBm
Supply Current (Idd)		7			25			40		mA

** R_{BIAS} resistor value sets current. See adaptive biasing application note.*

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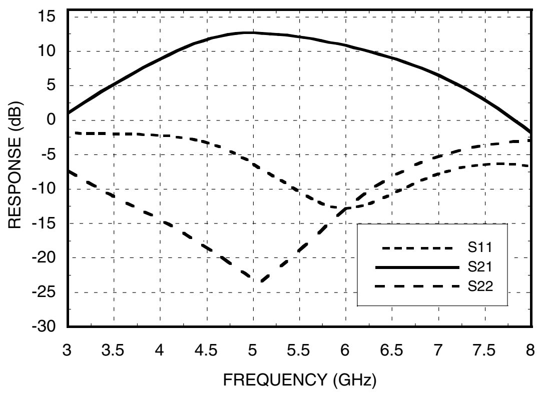
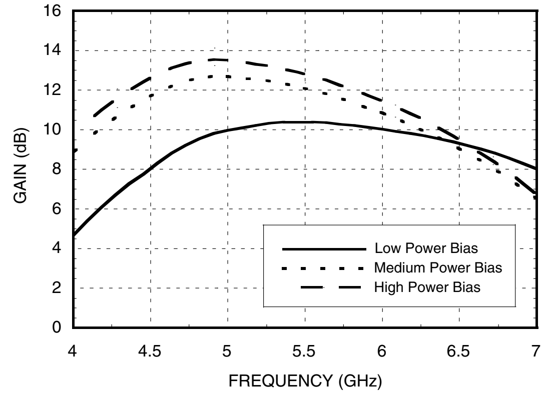
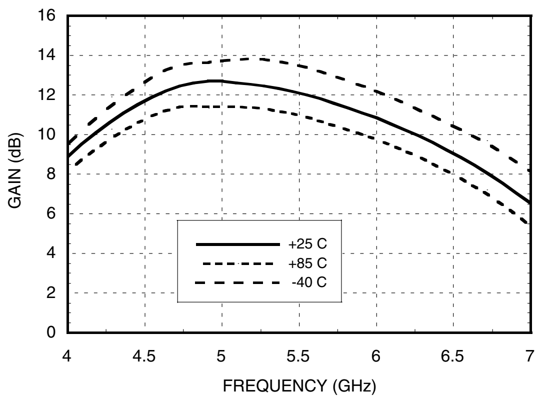
Broadband Gain & Return Loss Medium Power Bias



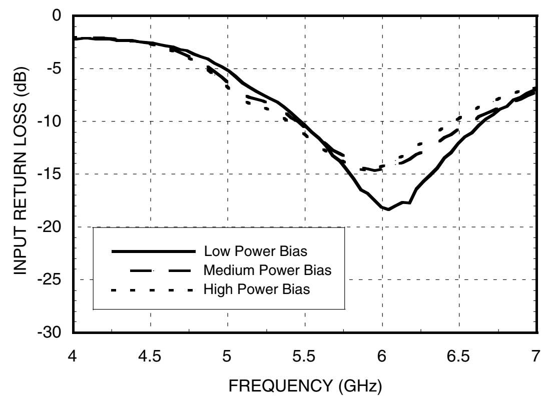
Gain @ Three Bias Conditions



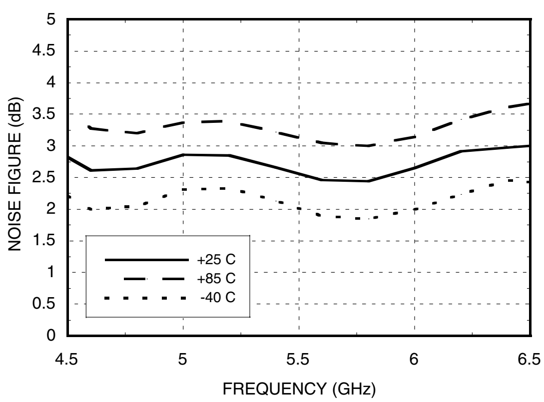
Gain vs. Temperature Medium Power Bias



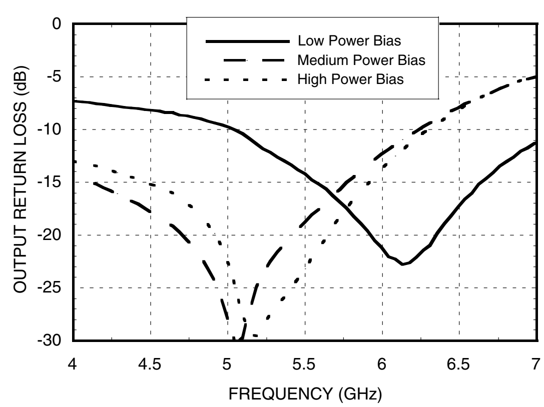
Input Return Loss @ Three Bias Conditions



Noise Figure vs. Temperature Medium Power Bias



Output Return Loss @ Three Bias Conditions



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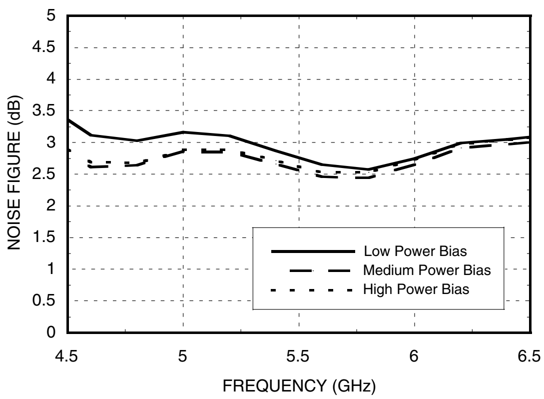
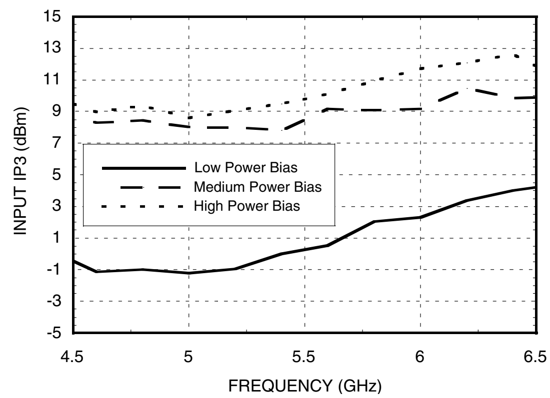
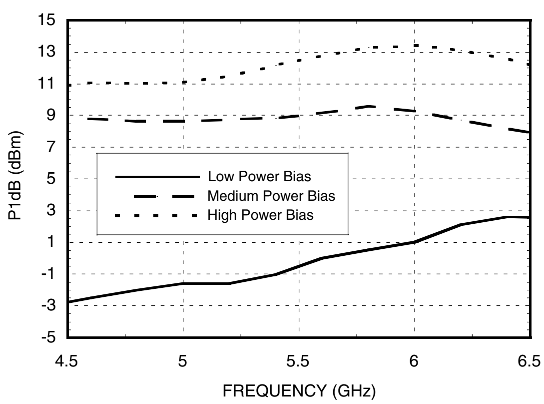
Noise Figure @ Three Bias Conditions



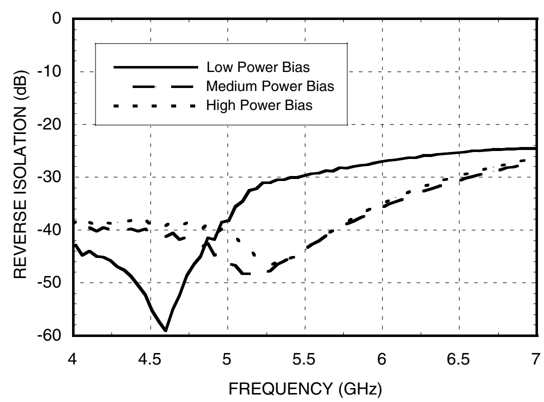
Input IP3 @ Three Bias Conditions



Output 1dB Compression @ Three Bias Conditions



Reverse Isolation @ Three Bias Conditions



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Adaptive Biasing

Optimizing P1dB Performance

The bias level may be changed to adjust the P1dB and return loss performance. The table below contains the HMC320MS8G RF performance as a function of various VSET and RBIAS settings. It will be necessary for the VSET voltage source to provide 100uA of current to the amplifier. The Idd and Vdd quiescent performance will not change as a function of changing the VSET voltage.

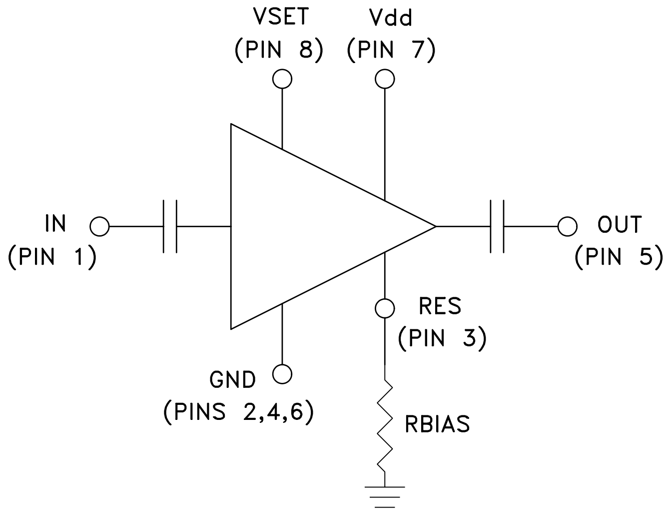
RF Performance at 5.8 GHz (Vdd = +3V)

VSET (VDC)	RBIAS Resistor Between Pin 3 and GND (Ohms)	Idd (mA)	Output P1dB (dBm)	Output Return Loss (dB)
0	174	7	1.0	16.0
3	23	25	9.0	12.0
3	7	40	13.0	15.0
3	GND (No Resistor)	60	14.0	15.0

Applying the adaptive biasing

A dynamically controlled bias can be implemented with this design. A typical application wil include sensing an RF signal level and then adjusting the VSET. The bias adjustment can be accomplished by either analog or digitals means, after the RF signal has been detected and translated to a DC voltage using external power detection circuitry.

Schematic



Absolute Maximum Ratings

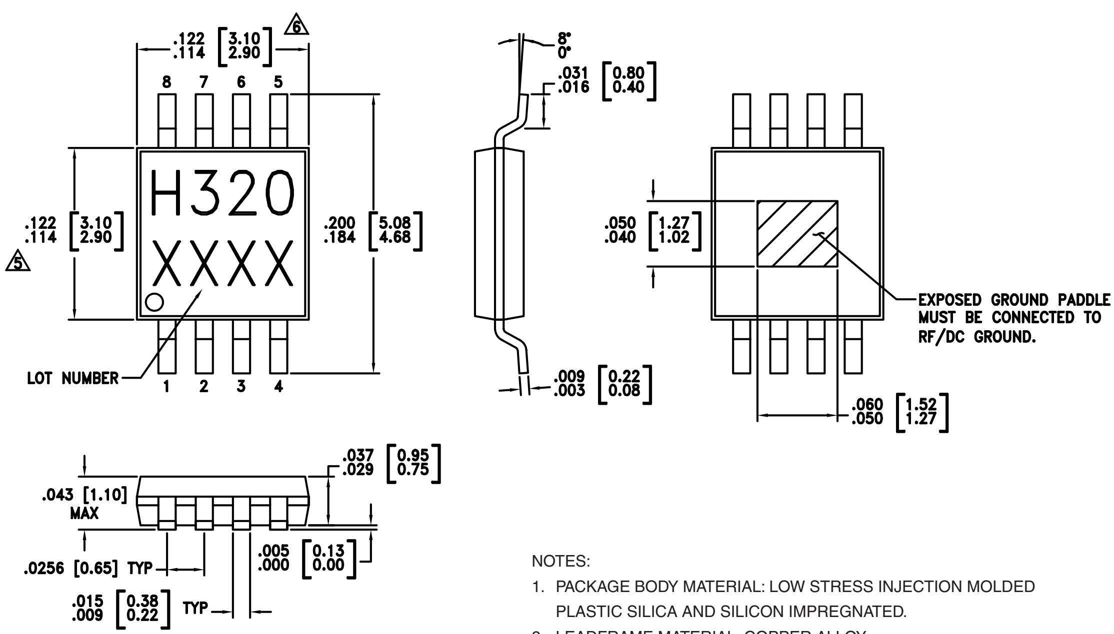
Drain Bias Voltage (Vdd)	+7.0 Vdc
Control Voltage Range (VSET)	0 to Vdd
RF Input Power (RFin)(Vdd = +3.0 Vdc)	+5 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 2.98 mW/°C above 85 °C)	0.194 W
Thermal Resistance (channel to ground paddle)	336 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Truth Table

VSET	Operating Current Idd	Operating State	Resistor Rbias
0V	7 mA	Low Power	174 Ohm
3V	25 mA	Medium Power	23 Ohm
3V	40 mA	High Power	7 Ohm

Set external bias resistor (R_{BIAS}) to achieve desired operating current, 0 < R_{BIAS} < 200 Ohm.

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEADFRAME MATERIAL: COPPER ALLOY
3. LEADFRAME PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

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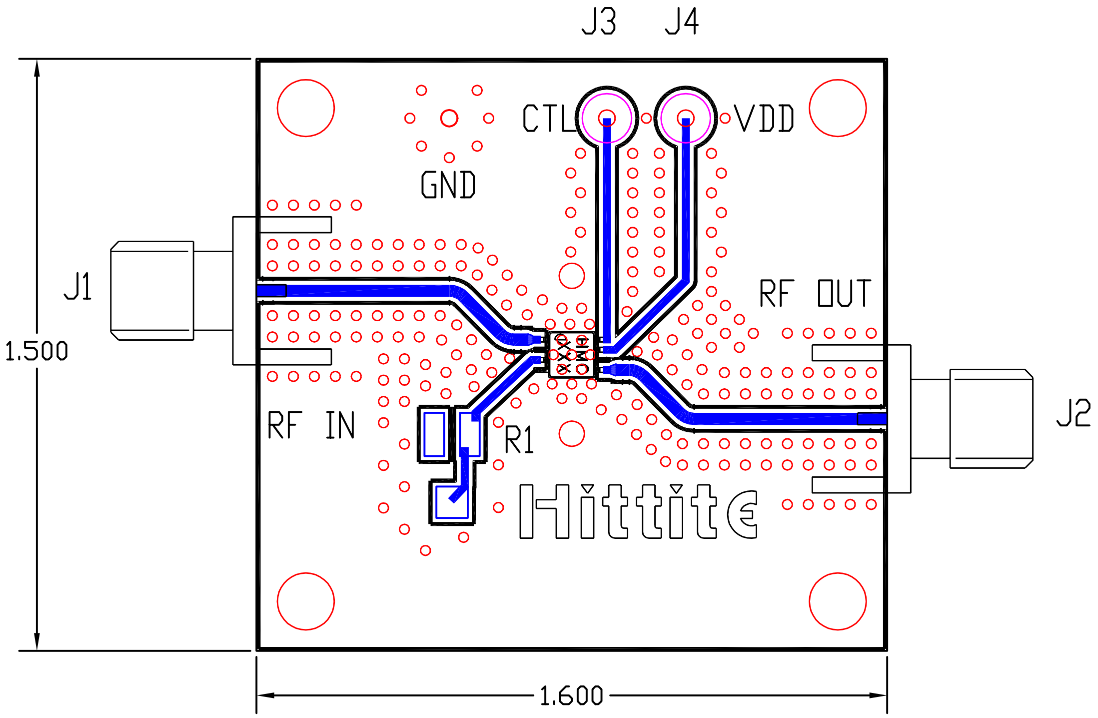
Evaluation PCB



List of Material

Item	Description
J1, J2	PC Mount SMA Connector
J3, J4	DC Pins
R1	200 Ohm Potentiometer
U1	HMC320MS8G Amplifier
PCB*	Evaluation PCB 1.6" x 1.5"
*Circuit Board Material: Rogers 4350	

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.